

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: Akira IMAI, et al.  
Application No.: TBD  
Filed: July 22, 2003  
For: MANUFACTURING METHOD OF SEMICONDUCTOR  
INTEGRATED CIRCUIT  
Exp. Art Group: 1765  
Exp. Examiner: William A. Powell

**CLAIM FOR PRIORITY**

Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

July 22, 2003

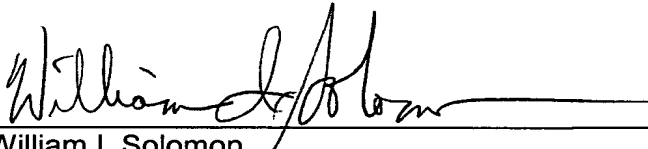
Sir:

Pursuant to the provisions of 35 USC §119 and 37 CFR § 1.55, Applicants hereby claim the right of priority based on Japanese Patent Application No. 2000-215093, filed in Japan on July 14, 2000.

A certified copy of the above-identified Japanese patent application was submitted on July 13, 2001, in prior Application No. 09/903,580, filed July 13, 2001.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

  
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WIS/sjg